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DATE: Friday, July 30, 2004

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<input type="checkbox"/>	L29	L28 and (gate or shifter or shift\$)	11
<input type="checkbox"/>	L28	L25 and (clock or cycle)	11
<input type="checkbox"/>	L27	L25 and (hash\$ same circuit\$)	4
<input type="checkbox"/>	L26	L25 and (logic same (gate or element))	6
<input type="checkbox"/>	L25	L24 and l18	17
<input type="checkbox"/>	L24	L23 and l10	82
<input type="checkbox"/>	L23	l11 and L22	149
<input type="checkbox"/>	L22	hash\$ same combinat\$	1958
<input type="checkbox"/>	L21	L17 and (structure same combinat\$)	72
<input type="checkbox"/>	L20	L17 and (structure same (nonsequen\$ or combinat\$))	72
<input type="checkbox"/>	L19	l17 and L18	5
<input type="checkbox"/>	L18	hash\$ same (structure or circuit)	4329
<input type="checkbox"/>	L17	L13 and (nonsequent\$ or combinat\$)	74
<input type="checkbox"/>	L16	L13 and (sequent\$ or combinat\$)	74
<input type="checkbox"/>	L15	l13 and L14	1
<input type="checkbox"/>	L14	hash\$ same (hdl or fpga or asic)	142
<input type="checkbox"/>	L13	L12 and multiplex\$ and decompos\$	74
<input type="checkbox"/>	L12	l10 and L11	154
<input type="checkbox"/>	L11	hash\$ and round\$3 and rout\$3 and (cryptograph\$ or cryptic)	523
<input type="checkbox"/>	L10	hash same (implementation or realiz\$)	1831
<input type="checkbox"/>	L9	L8 and decompos\$	4
<input type="checkbox"/>	L8	L3 not l7	85
<input type="checkbox"/>	L7	L6 and multiplex\$	30
<input type="checkbox"/>	L6	L4 and delay and propagat\$	30
<input type="checkbox"/>	L5	L4 and (fpga or asic or structure or architecture)	34
<input type="checkbox"/>	L4	L3 and combinat\$ and decompos\$	34
<input type="checkbox"/>	L3	hash\$ and round and rout\$ and (cryptograph or cryptic)	115
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<input type="checkbox"/>	L1	6594268	5

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 11 of 11 returned.

1. Document ID: US 20020032551 A1

Using default format because multiple data bases are involved.

L53: Entry 1 of 11

File: PGPB

Mar 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020032551

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020032551 A1

TITLE: Systems and methods for implementing hash algorithms

PUBLICATION-DATE: March 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Zakiya, Jabari	Hyattsville	MD	US	

US-CL-CURRENT: 703/2

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Sequences](#) [Attachments](#) [Claims](#) [KMC](#) [Draw. Desc](#) [Image](#)

2. Document ID: US 6701338 B2

L53: Entry 2 of 11

File: USPT

Mar 2, 2004

US-PAT-NO: 6701338

DOCUMENT-IDENTIFIER: US 6701338 B2

**** See image for Certificate of Correction ****

TITLE: Cumulative status of arithmetic operations

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Sequences](#) [Attachments](#) [Claims](#) [KMC](#) [Draw. Desc](#) [Image](#)

3. Document ID: US 6658556 B1

L53: Entry 3 of 11

File: USPT

Dec 2, 2003

US-PAT-NO: 6658556

DOCUMENT-IDENTIFIER: US 6658556 B1

TITLE: Hashing a target address for a memory access instruction in order to determine prior to execution which particular load/store unit processes the instruction

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Sequences](#) [Attachments](#) [Claims](#) [KMC](#) [Draw. Desc](#) [Image](#)

4. Document ID: US 6625689 B2

L53: Entry 4 of 11

File: USPT

Sep 23, 2003

US-PAT-NO: 6625689

DOCUMENT-IDENTIFIER: US 6625689 B2

**** See image for Certificate of Correction ****

TITLE: Multiple consumer-multiple producer rings

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Image](#) [Claims](#) [KOMC](#) [Draw. Desc](#) [Image](#)

5. Document ID: US 6598118 B1

L53: Entry 5 of 11

File: USPT

Jul 22, 2003

US-PAT-NO: 6598118

DOCUMENT-IDENTIFIER: US 6598118 B1

TITLE: Data processing system with HSA (hashed storage architecture)

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Image](#) [Claims](#) [KOMC](#) [Draw. Desc](#) [Image](#)

6. Document ID: US 6516404 B1

L53: Entry 6 of 11

File: USPT

Feb 4, 2003

US-PAT-NO: 6516404

DOCUMENT-IDENTIFIER: US 6516404 B1

**** See image for Certificate of Correction ****

TITLE: Data processing system having hashed architected processor facilities

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Image](#) [Claims](#) [KOMC](#) [Draw. Desc](#) [Image](#)

7. Document ID: US 6470442 B1

L53: Entry 7 of 11

File: USPT

Oct 22, 2002

US-PAT-NO: 6470442

DOCUMENT-IDENTIFIER: US 6470442 B1

TITLE: Processor assigning data to hardware partition based on selectable hash of data address

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Image](#) [Claims](#) [KOMC](#) [Draw. Desc](#) [Image](#)

8. Document ID: US 6449691 B1

L53: Entry 8 of 11

File: USPT

Sep 10, 2002

US-PAT-NO: 6449691

DOCUMENT-IDENTIFIER: US 6449691 B1

<http://westbirs:9000/bin/gate.exe?f=TOC&state=8agck0.121&ref=53&dbname=PGPB,USPT,JPAB&...> 7/30/04

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